EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Walter Kawula on November 6, 2009.

The application has been amended as follows:

Regarding Claim 1.

1. A circuit for converting frequency domain information to time domain information comprising:

a. an Inverse Fast Fourier Transform circuit having a length of N samples, the Inverse Fast Fourier Transform circuit adapted to receive input data of length N samples, to circularly shift the input data by m samples; and to generate output data of length N samples not multiplied by external rotator coefficients that are circularly shifted by m samples, where m is less than N; and

b. a Cyclical Prefix Insertion circuit adapted to insert a cyclical prefix of length m, the Cyclical Prefix Insertion circuit having;

1. a first switch, connected to the Inverse Fast Fourier Transform circuit;

2. a buffer, having an input connected to the first switch and an output, the buffer having a length m; and

3. a second switch, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the Inverse Fast Fourier Transform circuit to an output of the second switch[[.]]; wherein the N samples is a power of 2 and wherein the Inverse Fast Fourier Transform circuit implements an algorithm selected from the group consisting of Radix-2 and Radix-2^2 algorithms; and

wherein the Inverse Fast Fourier Transform circuit further comprises a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit, and the Inverse Fast Fourier Transform is adapted to circularly shift the input data by m samples by modifying memory contents for at least one multiplier circuit with memory and modifying the control for at least one rotator circuit.

Regarding Claim 3. Claim 3 is cancelled without prejudice.

Regarding Claim 4. Claim 4 is cancelled without prejudice.

Regarding Claim 5. Claim 5 is cancelled without prejudice.

Regarding Claim 6.

6. A circuit for converting frequency domain information to time domain information of ~~claim 3~~ claim 1 wherein the Inverse Fast Fourier Transform circuit ~~further comprises~~:

a. ~~a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits and coupled to an input,~~ wherein each butterfly circuit is configured to perform an addition operation and a subtraction operation;

b. [[a]] wherein the control circuit is configured to modify the control to the rotator circuit and to

selectively control the plurality of butterfly circuits whether the addition operation or the subtraction operation is output first in time to effect a circular shift of the output of the Inverse Fast Fourier Transform circuit by m samples; and

c. wherein the contents of the memory of the multiplier circuit with memory are arranged in a suitably modified manner.

Regarding Claim 7,

7. The circuit for converting frequency domain information to time domain information of ~~claim 3~~ claim 1 wherein the length of N samples is segmented into first, second, third, and fourth segments of N/4 samples, wherein the circular shift m is equal to N/4 and is effected by multiplying the input N samples by unity for the first segment of N/4 samples, -1 for the second segment of N/4 samples, -j for the third segment of N/4 samples, and j for the fourth segment of N/4 samples.

Regarding Claim 10,

10. The circuit for converting frequency domain information to time domain information of ~~claim 3~~ claim 1 wherein the length of N samples of the Inverse

Fast Fourier Transform and the cyclical prefix has a length m equal to N/4, and a control for a first rotator circuit is modified to effect the shift of the samples at the output of the Inverse Fast Fourier Transform by m samples.

Regarding claim 13,

13. A circuit for converting frequency domain information to time domain information comprising;

a. an Inverse Fast Fourier Transform circuit having:

1. an input adapted to receive frequency domain information;

2. an output providing time domain information;

3. the Inverse Fast Fourier Transform circuit having a length of N samples, where N is a power of 2 and the N samples are not multiplied by external rotator coefficients, and implementing an algorithm selected from the group consisting of Radix-2 and Radix-22 algorithms, the Inverse Fast Fourier Transform circuit further having a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a control circuit and configured to circularly shift output information by m samples, where m is less than N; and

b. guard interval insertion circuit adapted to insert a cyclical prefix of length m, the guard interval insertion circuit having;

1. a first switch, connected to the output of the Inverse Fast Fourier Transform circuit;

2. a buffer, having an input connected to the first switch and an output, the buffer having a length m; and

3. a second switch, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the output of the Inverse Fast Fourier Transform circuit to an output of the second switch.

Regarding Claim 17,

17. A circuit for converting frequency domain information to time domain information comprising:

a. a means for performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information to generate time domain information comprising a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit and a means for modifying the order of the contents of the memory for at least one multiplier circuit with memory and modifying the control circuit to modify the control for at least one rotator circuit and butterfly circuit, wherein the circular shift is approximately the same as a desired cyclical prefix and input samples for the Inverse Fast Fourier Transform are not multiplied by external rotator coefficients;

b. a first switch, connected to the means for performing a circularly rotated Inverse Fast Fourier Transform;

c. a means for buffering a portion of the time domain signals approximately the same as the desired cyclical prefix, the means for buffering having an input connected to the first switch; and

d. a second switch, coupled to the first switch and to the means for buffering, wherein the first and second switches selectively couple the output of the means for buffering and the means for performing a circularly rotated Inverse Fast Fourier Transform circuit to an output of the second switch.

Regarding Claim 19. Claim 19 is cancelled without prejudice.

Regarding Claim 20. Claim 20 is cancelled without prejudice.

Regarding Claim 22.

22. A method of generating circularly shifted time domain signal from frequency domain information in an Inverse Fast Fourier Transform circuit and having a desired cyclical prefix comprising:

a. performing a circularly rotated Inverse Fast Fourier Transform on frequency domain information to generate time domain information without multiplying input samples by external rotator coefficients, wherein the amount of the circular shift is the same as the length of the cyclical prefix, and wherein the Inverse Fast Fourier Transform comprises a plurality of butterfly circuits, rotator circuits and multiplier circuits

with memories, all coupled to a control circuit and the step of performing a circularly shifted Inverse Fast Fourier Transform further comprises modifying the control circuit to modify the control for at least one rotator circuit and butterfly circuit and memory contents of at least one multiplier circuit with memory;

b. storing the time domain information for a number of clock cycles equal to the cyclical prefix in a buffer while simultaneously outputting the time domain information;

c. outputting the time domain information for a number of clock cycles equal to a length of the Inverse Fast Fourier Transform minus the length of the cyclical prefix; and

d. outputting the time domain information stored in the buffer for a number of clock cycles equal to the length of the cyclical prefix.

Regarding Claim 24. Claim 24 is cancelled without prejudice.

Regarding Claim 25. Claim 25 is cancelled without prejudice.

Regarding Claim 26. Claim 26 is cancelled without prejudice.

Regarding Claim 27. Claim 27 is cancelled without prejudice.

Regarding Claim 28. Claim 28 is cancelled without prejudice.

Regarding Claim 29, Claim 29 is cancelled without prejudice.

Regarding Claim 30, Claim 30 is cancelled without prejudice.

Regarding Claim 31, Claim 31 is cancelled without prejudice.

Regarding Claim 32, Claim 32 is cancelled without prejudice.

Regarding Claim 33, Claim 33 is cancelled without prejudice.

2. The following is an examiner's statement of reasons for allowance:

Claims 1, 13, 17 and 22 are allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose **performing a circularly shifted Inverse Fast Fourier Transform on frequency domain information to generate time domain information comprising a plurality of butterfly circuits, rotator circuits and multiplier circuits with memories, all coupled to a control circuit and a means for modifying the order of the contents of the memory for at least one multiplier circuit with memory and modifying the control circuit to modify the control for at least one rotator circuit and butterfly circuit, wherein the circular shift is approximately the same as a desired cyclical prefix and input samples for the Inverse Fast Fourier Transform are not multiplied by**

external rotator coefficients. It is noted that the closest prior art, Yeh (US 2004/0059766) shows an IFFT circuit comprising a plurality of butterfly circuits and multipliers under the control of a control unit. However, Yeh fails to disclose or render obvious the above underlined limitations as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER P. GREY whose telephone number is (571)272-3160. The examiner can normally be reached on 10AM-7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Moe Aung can be reached on (571)272-7314. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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